1.8V Nanopower Comparator with Internal 1.245V Reference

FEATURES

- Second-source for MAX917
- Guaranteed to Operate Down to +1.8V
- Ultra-Low Supply Current: 750nA
- Internal 1.245V ±1.5% Reference
- Input Voltage Range Extends 200mV Outside-the-Rails
- No Phase Reversal for Overdriven Inputs
- Push-pull Output
- Crowbar-Current-Free Switching
- Internal Hysteresis for Clean Switching
- 5-pin SOT23 and 8-pin SOIC Packaging

APPLICATIONS

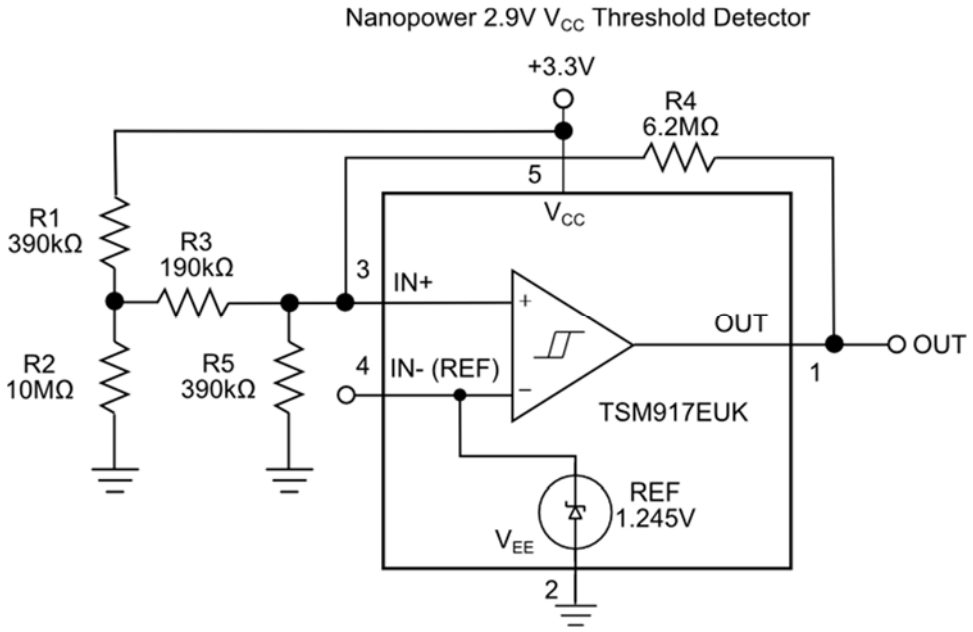
2-Cell Battery Monitoring/Management
Medical Instruments
Threshold Detectors/Discriminators
Sensing at Ground or Supply Line
Ultra-Low-Power Systems
Mobile Communications
Telemetry and Remote Systems

DESCRIPTION

The TSM917 nanopower analog comparator is electrically and form-factor identical to the MAX917 analog comparator. Ideally suited for all 2-cell battery-management/monitoring applications, this 5-pin SOT23 analog comparator guarantees +1.8V operation, draws very little supply current, and has a robust input stage that can tolerate input voltages beyond its power supply. The TSM917 draws 750nA of supply current and includes an on-board 1.245V ±1.5% reference.

The TSM917's push-pull output drivers were designed to drive 8mA loads from one supply rail to the other supply rail. The TSM917 is also available in an 8-pin SOIC package.

TYPICAL APPLICATION CIRCUIT



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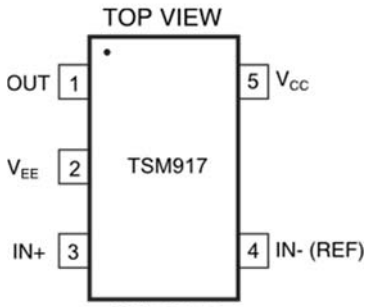
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) ..... +6V
Voltage Inputs (IN+, IN-, REF) .... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Voltage
TSM917 ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Current Into Input Pins ..... ±20mA
Output Current ..... ±50mA
Output Short-Circuit Duration 10s

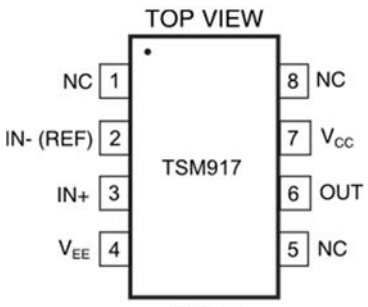
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (Derate 2.5mW/°C above +70°C) 200mW
8-Pin SOIC (Derate 5.88mW/°C above +70°C) 471mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



SOT23-5
UK Package



SO-8
SA Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM917EUK+	TAAA	Tape & Reel	-----	TSM917ESA+	TS917E	Tube	97
TSM917EUK+T		Tape & Reel	3000	TSM917ESA+T		Tape & Reel	2500

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = V_{REF}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Note 1.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from the PSRR test	T_A = +25°C	1.8		5.5	V
Supply Current	I_{CC}	V_{CC} = 1.6V	T_A = +25°C		0.75		µA
		V_{CC} = 5V	T_A = +25°C		0.80	1.30	
			T_A = T_{MIN} to T_{MAX}			1.60	
IN+ Voltage Range	V_{IN+}	Inferred from the output swing test		V_{EE} - 0.2		V_{CC} + 0.2	V
Input Offset Voltage	V_{OS}	(Note 2)	T_A = +25°C		1	5	mV
			T_A = T_{MIN} to T_{MAX}			10	
Input-Referred Hysteresis	V_{HB}	(Note 3)			4		mV
Input Bias Current	I_B	T_A = +25°C			0.15	1	nA
		T_A = T_{MIN} to T_{MAX}				2	
Power-Supply Rejection Ratio	PSRR	V_{CC} = 1.8V to 5.5V			0.1	1	mV/V
Output-Voltage Swing High	V_{CC} - V_{OH}	V_{CC} = 5V, I_{SOURCE} = 8mA	T_A = +25°C		190	400	mV
			T_A = T_{MIN} to T_{MAX}			500	
		V_{CC} = 1.8V, I_{SOURCE} = 1mA	T_A = +25°C		55	200	
			T_A = T_{MIN} to T_{MAX}			300	
Output-Voltage Swing Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 8mA	T_A = +25°C		190	400	mV
			T_A = T_{MIN} to T_{MAX}			500	
		V_{CC} = 1.8V, I_{SINK} = 1mA	T_A = +25°C		55	200	
			T_A = T_{MIN} to T_{MAX}			300	
Output Short-Circuit Current	I_{SC}	Sourcing, V_O = V_{EE}	V_{CC} = 5V		95		mA
			V_{CC} = 1.8V		8		
		Sinking, V_O = V_{CC}	V_{CC} = 5V		98		
			V_{CC} = 1.8V		10		
High-to-Low Propagation Delay (Note 4)	t_{PD-}	V_{CC} = 1.8V			17		µs
		V_{CC} = 5V			22		
Low-to-High Propagation Delay (Note 4)	t_{PD+}		V_{CC} = 1.8V		30		µs
			V_{CC} = 5V		95		
Rise Time	t_{RISE}	C_L = 15pF			6		µs
Fall Time	t_{FALL}	C_L = 15pF			4		µs
Power-Up Time	t_{ON}				1.2		ms
Reference Voltage	V_{REF}	T_A = +25°C		1.227	1.245	1.263	V
		T_A = T_{MIN} to T_{MAX}		1.200		1.290	
Reference Voltage Temperature Coefficient	TCV_{REF}				95		ppm/°C
Reference Output Voltage Noise	e_n	BW = 10Hz to 100kHz			600		$µV_{RMS}$
		BW = 10Hz to 100kHz, C_{REF} = 1nF			215		
Reference Line Regulation	$\Delta V_{REF}/\Delta V_{CC}$	V_{CC} = 1.8V to 5.5V			0.1		mV/V
Reference Load Regulation	$\Delta V_{REF}/\Delta I_{OUT}$	ΔI_{OUT} = 10nA			±0.2		mV/nA

Note 1: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by design, not production tested.

Note 2: V_{OS} is defined as the center of the hysteresis band at the input.

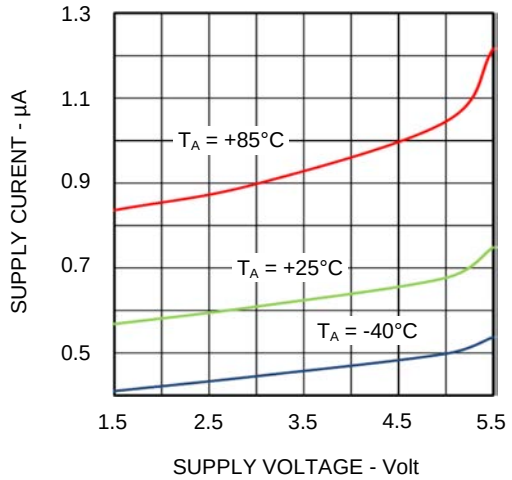
Note 3: The hysteresis-related trip points are defined by the edges of the hysteresis band, measured with respect to the center of the hysteresis band (i.e., V_{OS}) (See Figure 2).

Note 4: Specified with an input overdrive ($V_{OVERDRIVE}$) of 100mV, and load capacitance of C_L = 15pF. $V_{OVERDRIVE}$ is defined above and beyond the offset voltage and hysteresis of the comparator input. For the TSM917, reference voltage error should also be added.

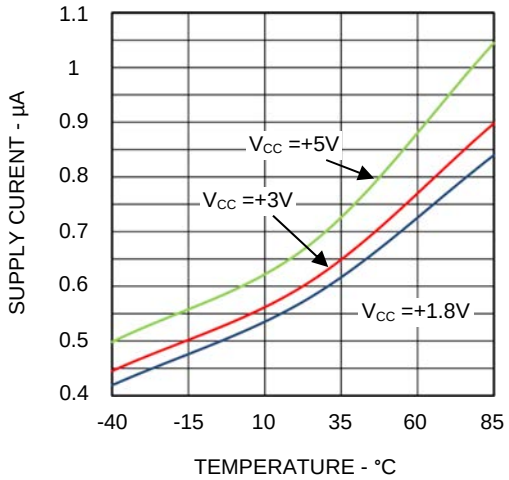
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

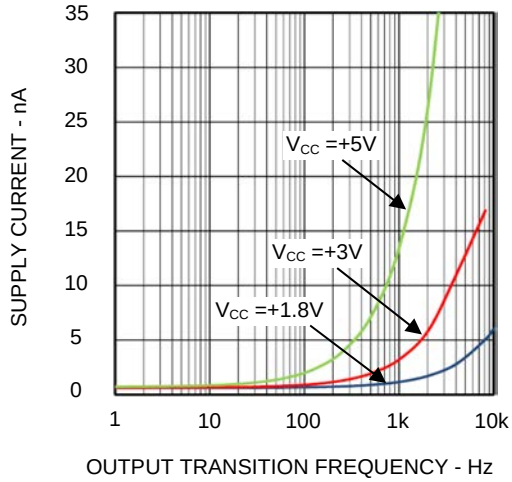
Supply Current vs Supply Voltage and Temperature



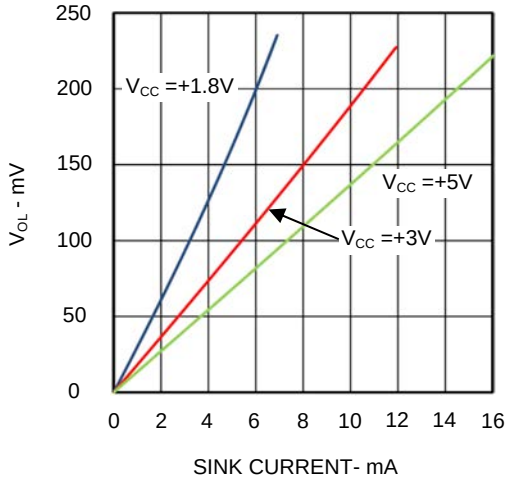
Supply Current vs Temperature



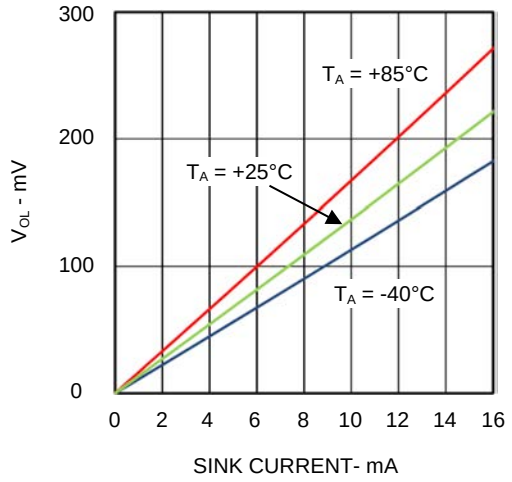
Supply Current vs Output Transition Frequency



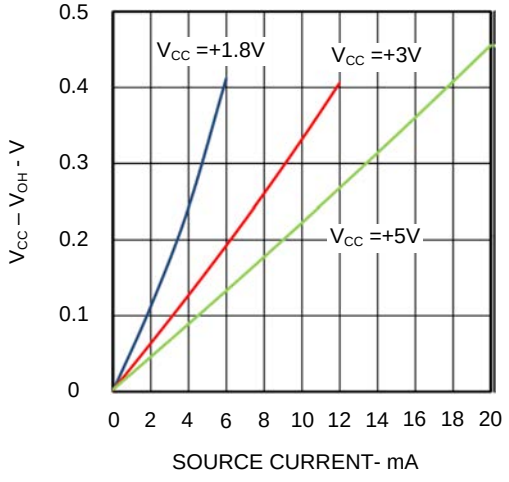
Output Voltage Low vs. Sink Current



Output Voltage Low vs. Sink Current and Temperature



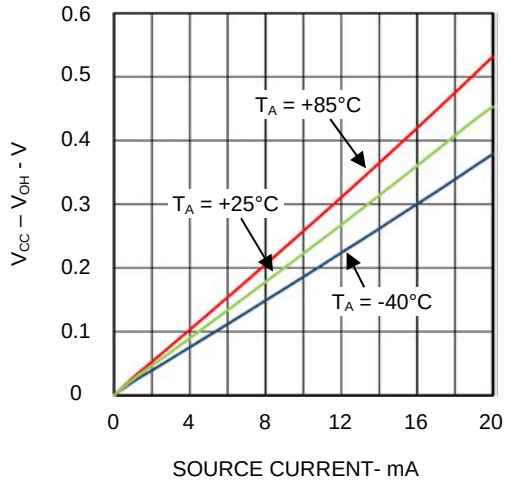
Output Voltage High vs Source Current



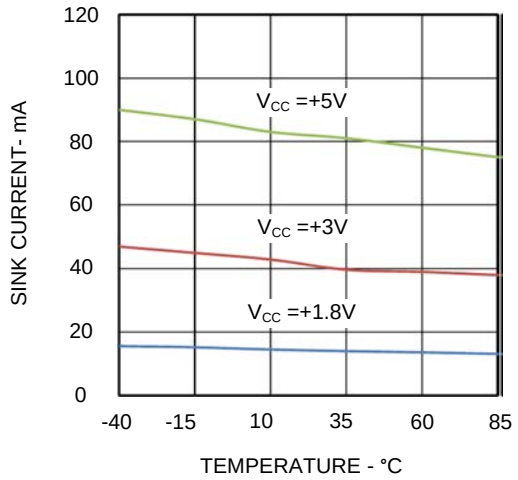
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

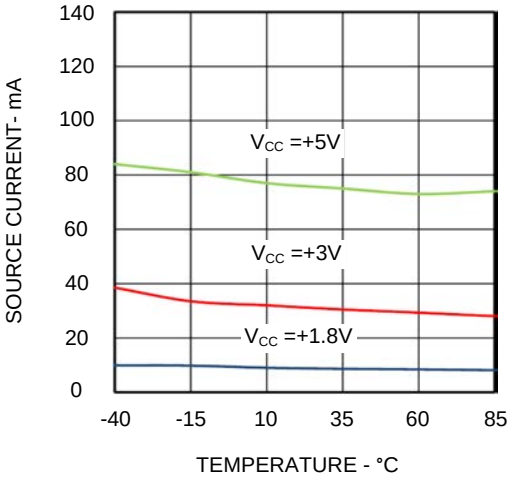
Output Voltage High vs Source Current and Temperature



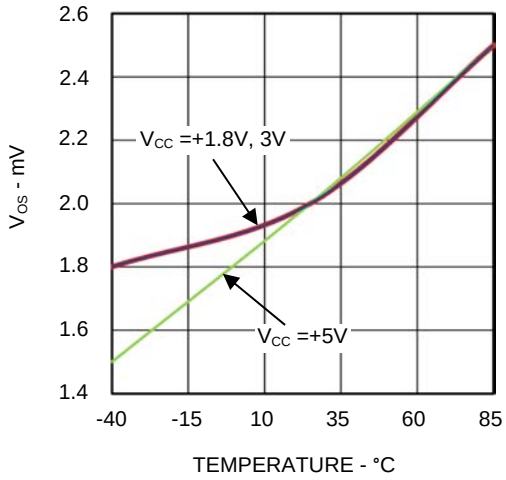
Short-Circuit Sink Current vs Temperature



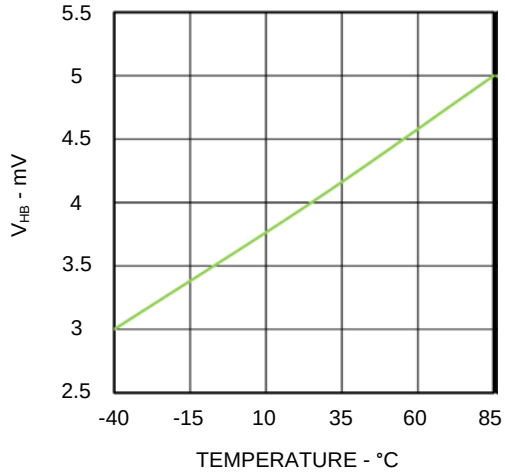
Short-Circuit Source Current vs Temperature



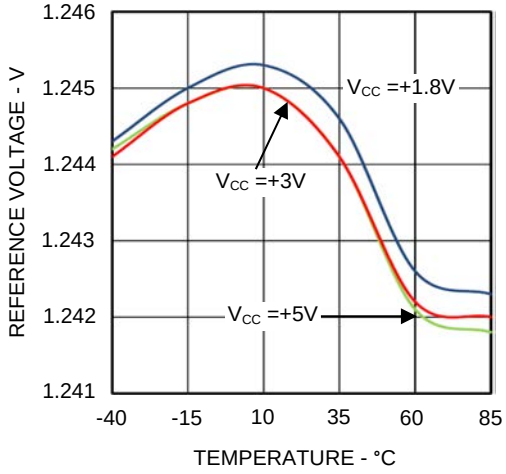
Offset Voltage vs Temperature



Hysteresis Voltage vs Temperature



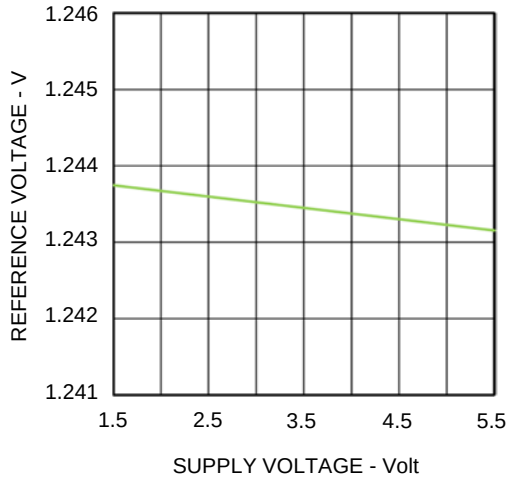
Reference Voltage vs Temperature



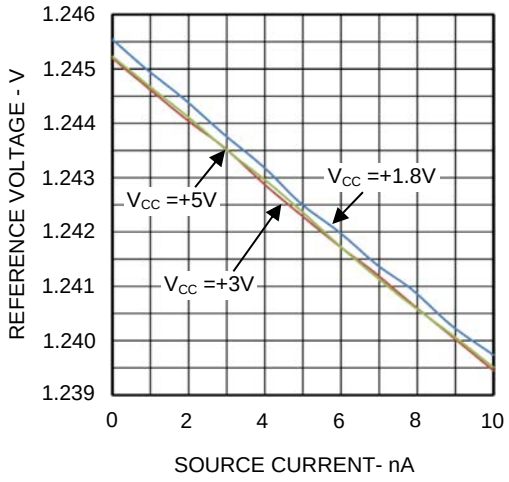
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

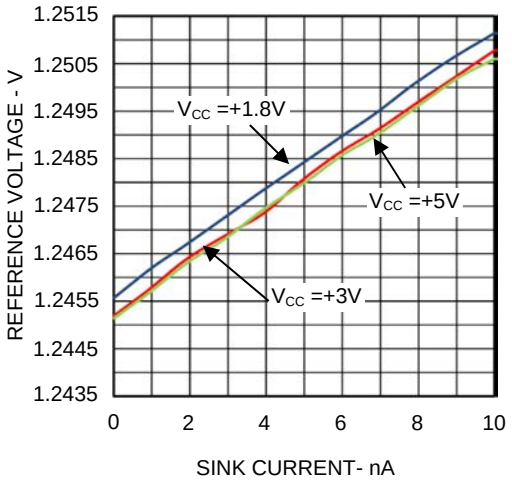
Reference Voltage vs Supply Voltage



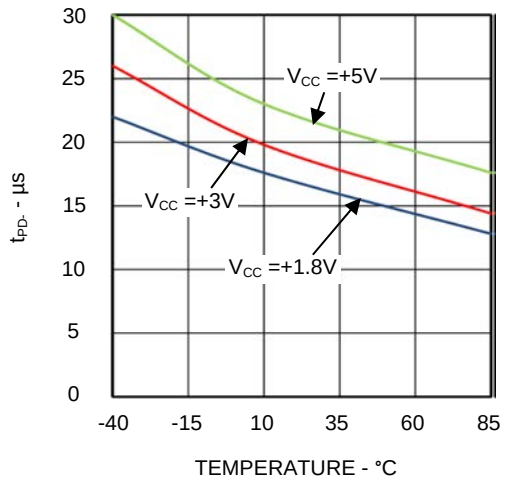
Reference Voltage vs Reference Source Current



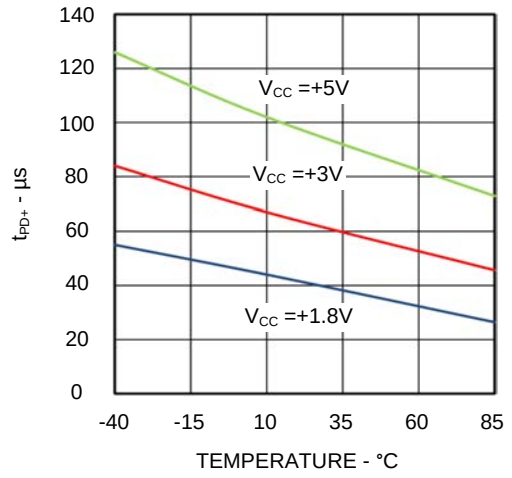
Reference Voltage vs Reference Sink Current



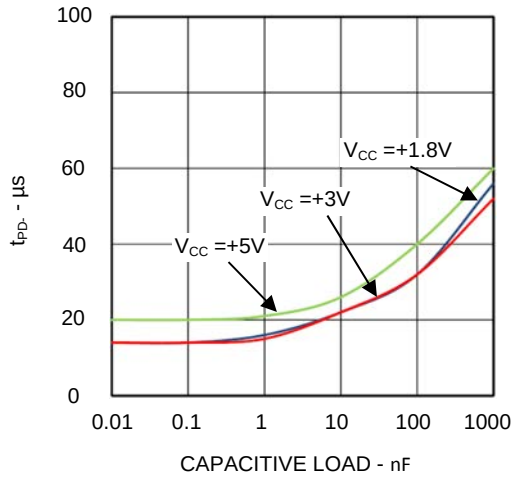
Propagation Delay (t_{PD-}) vs Temperature



Propagation Delay (t_{PD+}) vs Temperature



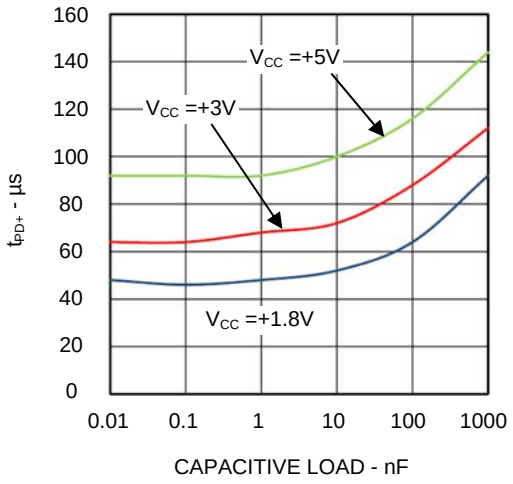
Propagation Delay (t_{PD-}) vs Capacitive Load



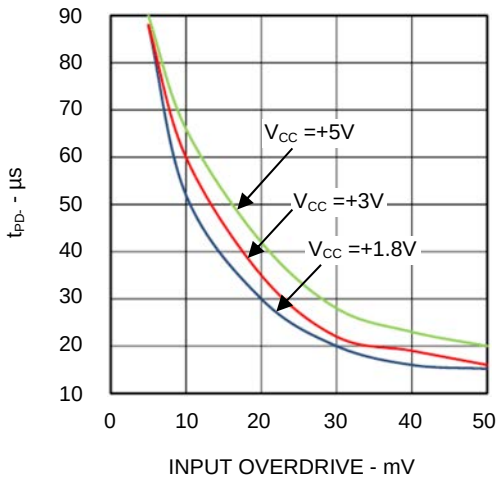
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

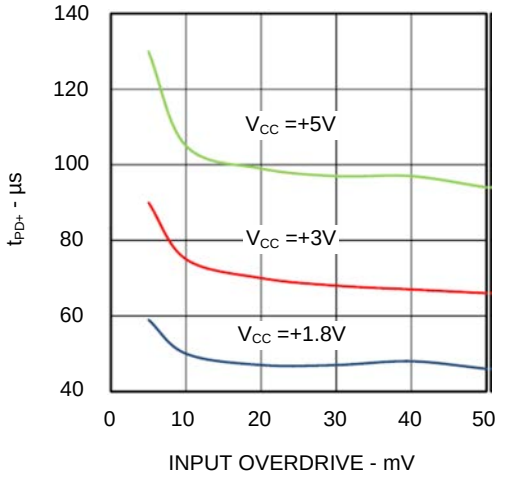
Propagation Delay (t_{PD+}) vs Capacitive Load



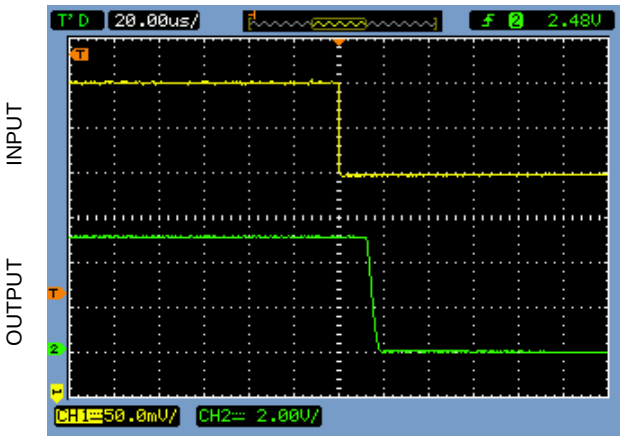
Propagation Delay (t_{PD-}) vs Input Overdrive



Propagation Delay (t_{PD+}) vs Input Overdrive

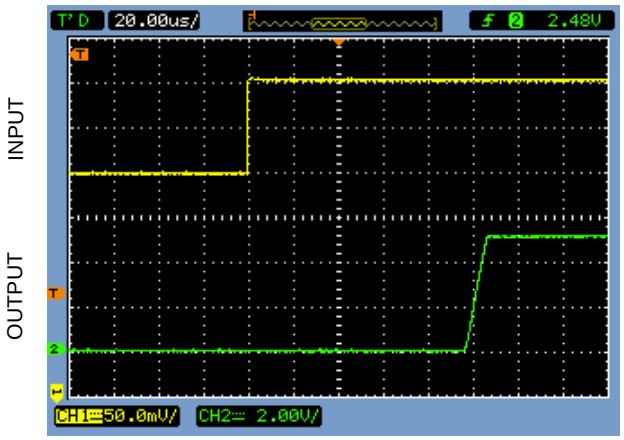


Propagation Delay (t_{PD-}) at V_{CC} = +5V



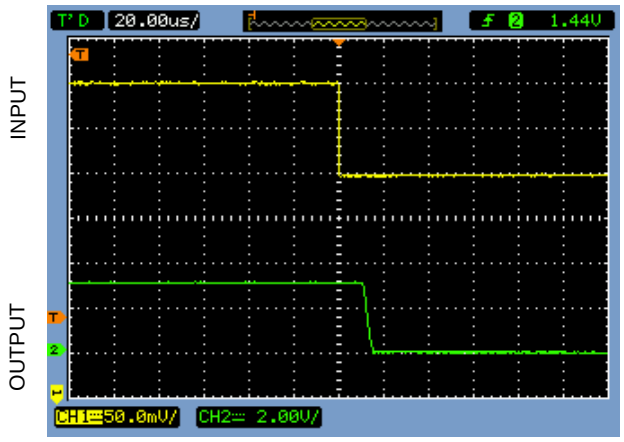
20µs/DIV

Propagation Delay (t_{PD+}) at V_{CC} = +5V



20µs/DIV

Propagation Delay (t_{PD-}) at V_{CC} = +3V

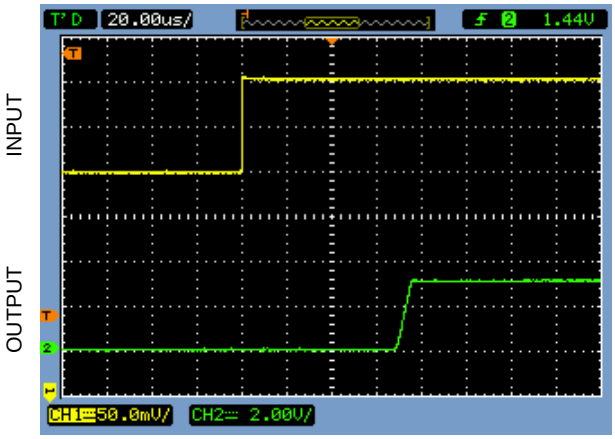


20µs/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

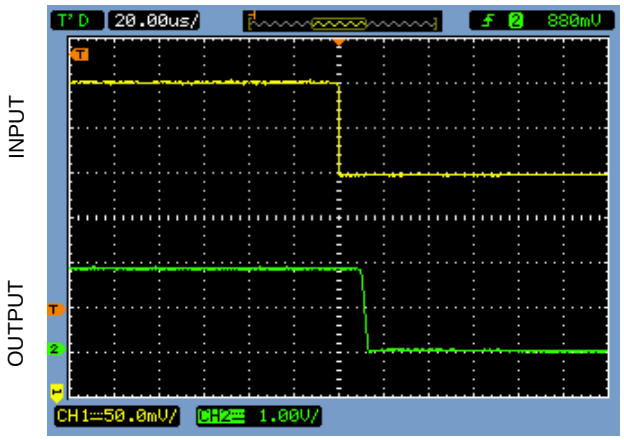
V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

Propagation Delay (t_{PD+}) at V_{CC} = +3V



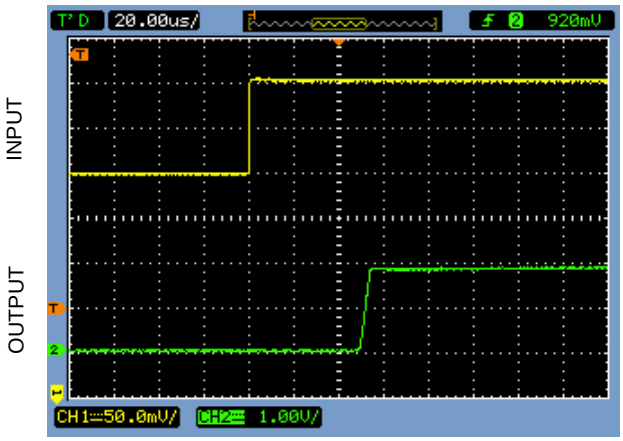
20µs/DIV

Propagation Delay (t_{PD-}) at V_{CC} = +1.8V



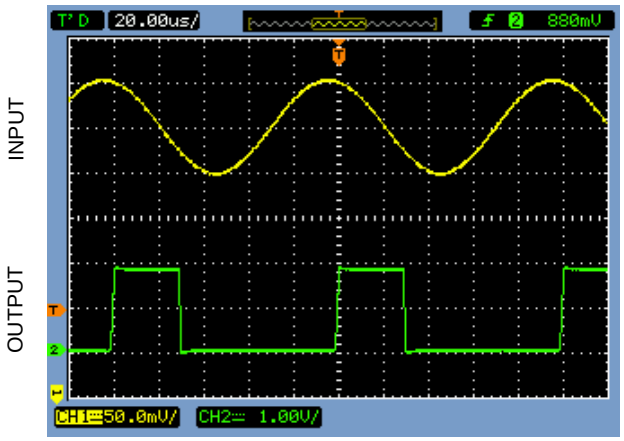
20µs/DIV

Propagation Delay (t_{PD+}) at V_{CC} = +1.8V



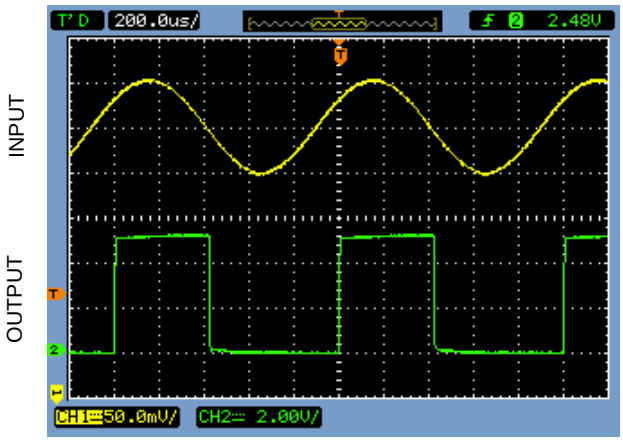
20µs/DIV

10kHz Transient Response at V_{CC} = +1.8V



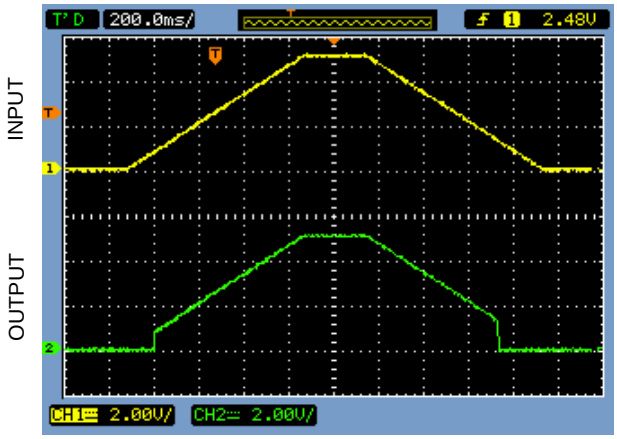
20µs/DIV

1kHz Transient Response at V_{CC} = +5V



200µs/DIV

Power-Up/Power-Down Transient Response

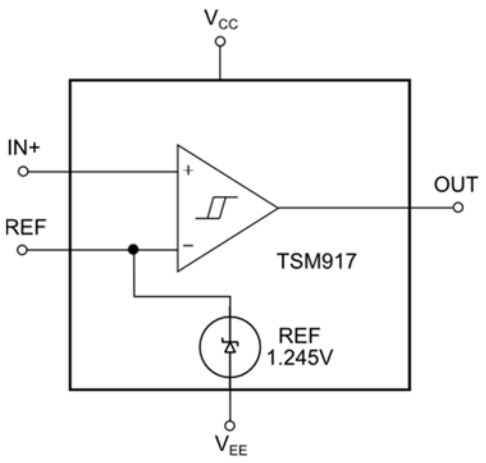


0.2s/DIV

PIN FUNCTIONS

TSM917		NAME	FUNCTION
5-pin SOT23	8-pin SOIC		
1	6	OUT	Comparator Output
2	4	VEE	Negative Supply Voltage
3	3	IN+	Comparator Noninverting Input
4	2	REF	1.245V Reference Output and Comparator Inverting Input
5	7	VCC	Positive Supply Voltage
—	—	IN-	Comparator Inverting Input
—	1, 5, 8	NC	No Connection. Not internally connected.

BLOCK DIAGRAMS



DESCRIPTION OF OPERATION

Guaranteed to operate from +1.8V supplies, the TSM917 analog comparator only draws 750nA supply current, features a robust input stage that can tolerate input voltages 200mV beyond the power supply rails, and includes an on-board +1.245V ±1.5% voltage reference. To insure clean output switching behavior, the TSM917 features 4mV internal hysteresis. The TSM917's push-pull output drivers were designed to minimize supply-current surges while driving ±8mA loads with rail-to-rail output swings.

Input Stage Circuitry

The robust design of the analog comparator's input stage can accommodate any differential input voltage from V_{EE} - 0.2V to V_{CC} + 0.2V. Input bias currents are typically ±0.15nA so long as the applied input voltage remains between the supply rails. ESD protection diodes - connected internally to the supply rails - protect comparator inputs against overvoltage conditions. However, if the applied input voltage exceeds either or both supply rails, an increase in input current can occur when these ESD protection diodes start to conduct.

Output Stage Circuitry

Many conventional analog comparators can draw orders of magnitude higher supply current when switching. Because of this behavior, additional power supply bypass capacitance may be required to provide additional charge storage during switching. The design of the TSM917's rail-to-rail output stage implements a technique that virtually eliminates supply-current surges when output transitions occur. As shown on Page 4 of the Typical Operating Characteristics, the supply-current change as a function of output transition frequency exhibited by this analog comparator family is very small. Material benefits of this attribute to battery-power applications are the increase in operating time and in reducing the size of power-supply filter capacitors.

TSM917's Internal +1.245V V_{REF}

The TSM917's internal +1.245V voltage reference exhibits a typical temperature coefficient of 95ppm/°C over the full -40°C to +85°C temperature range. An equivalent circuit for the reference section is illustrated in Figure 1. Since the output impedance of the voltage reference is typically 200kΩ, its output can be bypassed with a low-leakage capacitor and is stable for any capacitive load. An external buffer – such as the TS1001 – can be used to buffer the voltage reference output for higher output current drive or to reduce reference output impedance.

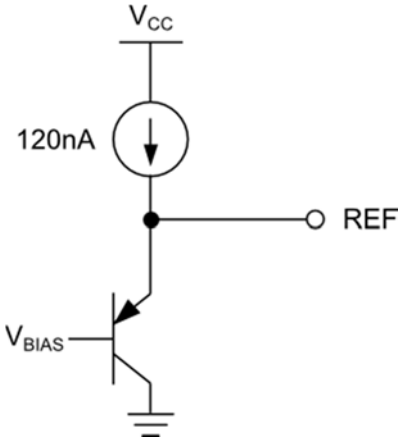


Figure 1: TSM917's Internal V_{REF} Output Equivalent Circuit

APPLICATIONS INFORMATION

Low-Voltage, Low-Power Operation

Because it was designed specifically for any low-power, battery-operated application, the TSM917 analog comparator is an excellent choice. Under nominal conditions, approximate operating times for this analog comparator is illustrated in Table 1 for a number of battery types and their corresponding charge capacities.

Internal Hysteresis

As a result of circuit noise or unintended parasitic feedback, many analog comparators often break into oscillation within their linear region of operation especially when the applied differential input voltage approaches 0V (zero volt). Externally-introduced hysteresis is a well-established technique to stabilizing analog comparator behavior and requires external components. As shown in Figure 2, adding comparator hysteresis creates two trip points: V_{THR} (for the rising input voltage) and V_{THF} (for the falling input voltage). The hysteresis band (V_{HB}) is defined as the voltage difference between the two trip points. When a comparator's input voltages are equal, hysteresis effectively forces one comparator input to

Table 1: Battery Applications using the TSM917

BATTERY TYPE	RECHARGEABLE	V_{FRESH} (V)	$V_{END\text{-}OF\text{-}LIFE}$ (V)	CAPACITY, AA SIZE (mA-h)	TSM917 OPERATING TIME (hrs)
Alkaline (2 Cells)	No	3.0	1.8	2000	2.5×10^6
Nickel-Cadmium (2 Cells)	Yes	2.4	1.8	750	937,500
Lithium-Ion (1 Cell)	Yes	3.5	2.7	1000	1.25×10^6
Nickel-Metal- Hydride (2 Cells)	Yes	2.4	1.8	1000	1.25×10^6

move quickly past the other input, moving the input out of the region where oscillation occurs. Figure 2 illustrates the case in which an IN- input is a fixed voltage and an IN+ is varied. If the input signals were reversed, the figure would be the same with an inverted output. To save cost and external pcb area, an internal 4mV hysteresis circuit was added to the TSM917.

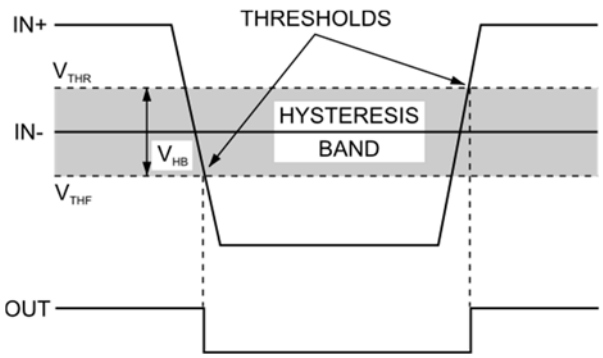


Figure 2: TSM917's Threshold Hysteresis Band

Adding Hysteresis to the TSM917

The TSM917 exhibits an internal hysteresis band (V_{HB}) of 4mV. Additional hysteresis can be generated with three external resistors using positive feedbackas shown in Figure 3. Unfortunately, this method also reduces the hysteresis response time. The design procedure below can be used to calculate resistor values.

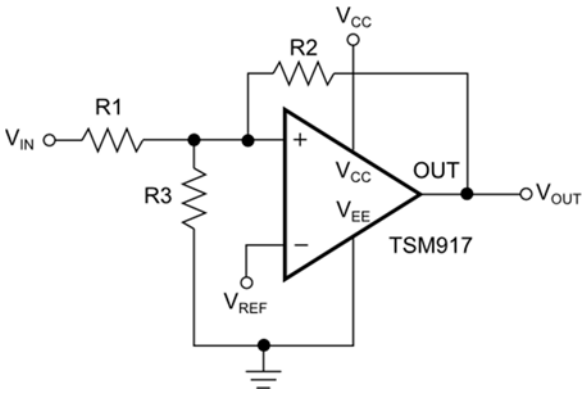


Figure 3: Using Three Resistors Introduces Additional Hysteresis in the TSM917.

1) Setting R2. As the leakage current at the IN pin is under 2nA, the current through R2 should be at least 0.2µA to minimize offset voltage errors caused by the input leakage current. The current through R2 at the trip point is (V_{REF} - V_{OUT})/R2.

   In solving for R2, there are two formulas – one each for the two possible output states:

   $R2 = V_{REF}/I_{R2}$

   or

   $R2 = (V_{CC} - V_{REF})/I_{R2}$

   From the results of the two formulae, the smaller of the two resulting resistor values is chosen. For example, when using the TSM917 (V_{REF} = 1.245V) at a V_{CC} = 3.3V and if I_{R2} = 0.2µA is chosen, then the formulae above produce two resistor values: 6.23MΩ and 10.24MΩ - the 6.2MΩ standard value for R2 is selected.

2) Next, the desired hysteresis band (V_{HYSB}) is set. In this example, V_{HYSB} is set to 100mV.

3) Resistor R1 is calculated according to the following equation:

   $R1 = R2 \times (V_{HB}/V_{CC})$

   and substituting the values selected in 1) and 2) above yields:

   R1 = 6.2MΩ x (100mV/3.3V) = 187.88kΩ

   The 187kΩ standard value for R1 is selected.

4) The trip point for V_{IN} rising (V_{THR}) is chosen such that $V_{THR} > V_{REF} \times (R1 + R2)/R2$ (where V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. In this example, V_{THR} is set to 3V.

5) With the V_{THR} from Step 4 above, resistor R3 is then computed as follows:

   $R3 = 1/[V_{THR}/(V_{REF} \times R1) - (1/R1) - (1/R2)]$

   R3 = 1/[3V/(1.245V x 187kΩ) - (1/187kΩ) - (1/6.2MΩ)] = 135.56kΩ

   In this example, a 137kΩ, 1% standard value resistor is selected for R3.

6) The trip voltages and hysteresis band should be verified as follows:

   For V_{IN} rising: $V_{THR} = V_{REF} \times R1 \times [(1/R1) + (1 / R2) + (1 / R3)] = 3V$

   For V_{IN} falling: $V_{THF} = V_{THR} - (R1 \times V_{CC}/R2) = 2.9V$

   and Hysteresis Band = $V_{THR} – V_{THF}$ = 100mV

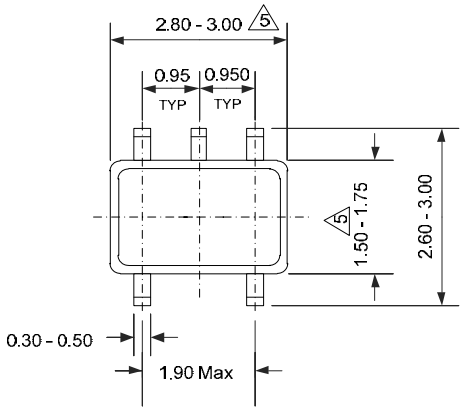
PC Board Layout and Power-Supply Bypassing

While power-supply bypass capacitors are not typically required, it is always good engineering practice to use 0.1uF bypass capacitors close to the device's power supply pins when the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

PACKAGE OUTLINE DRAWING

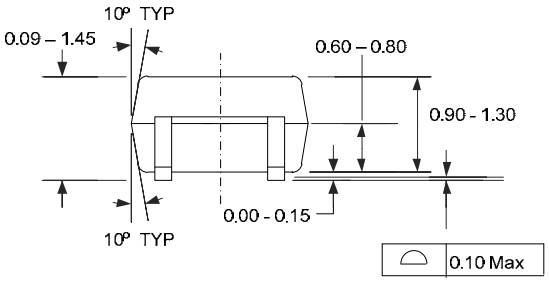
5-Pin SOT23 Package Outline Drawing

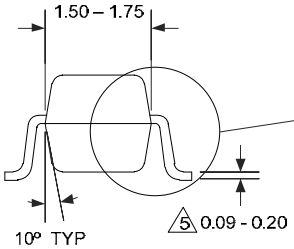
(N.B., Drawings are not to scale)

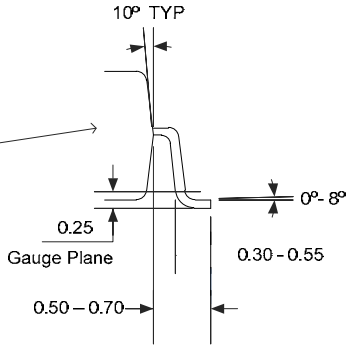


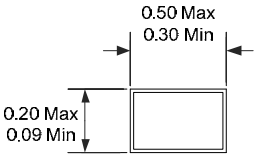
NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up mold and facing down for trim/form, ie, reverse trim/form.
4. The foot length measuring is based on the gauge plane method.
5. Dimensions are exclusive of mold flash and gate burr.
6. Dimensions are exclusive of solder plating.
7. All dimensions are in mm.
8. This part is compliant with EIAJ spec. and JEDEC MO-178 AA
9. Lead span/stand off height/coplanarity are considered as special characteristic.





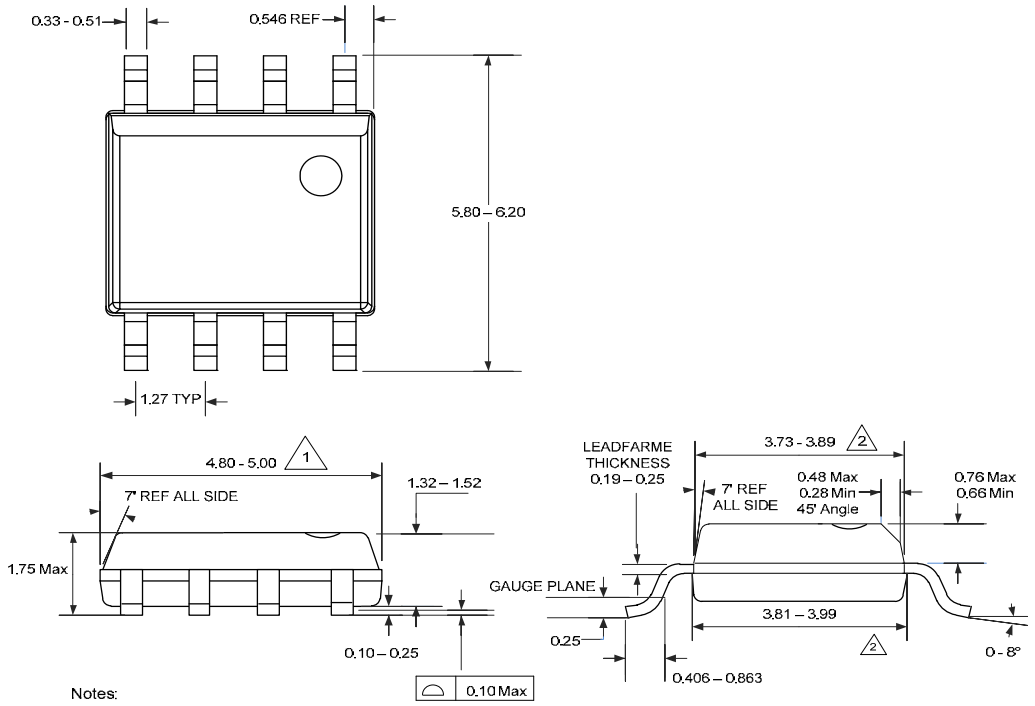




PACKAGE OUTLINE DRAWING

8-Pin SOIC Package Outline Drawing

(N.B., Drawings are not to scale)



Notes:

1. Does not include mold flash, protrusions or gate burns. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
2. Does not include inter-lead flash or protrusions. Inter-lead flash or protrusions shall not exceed 0.25 mm per side.
3. Lead span/stand off height/coplanarity are considered as special characteristic (S).
4. Controlling dimensions are in mm.
5. This part is compliant with JEDEC specification MS-012
6. Lead span/stand off height/coplanarity are considered as Special characteristic.

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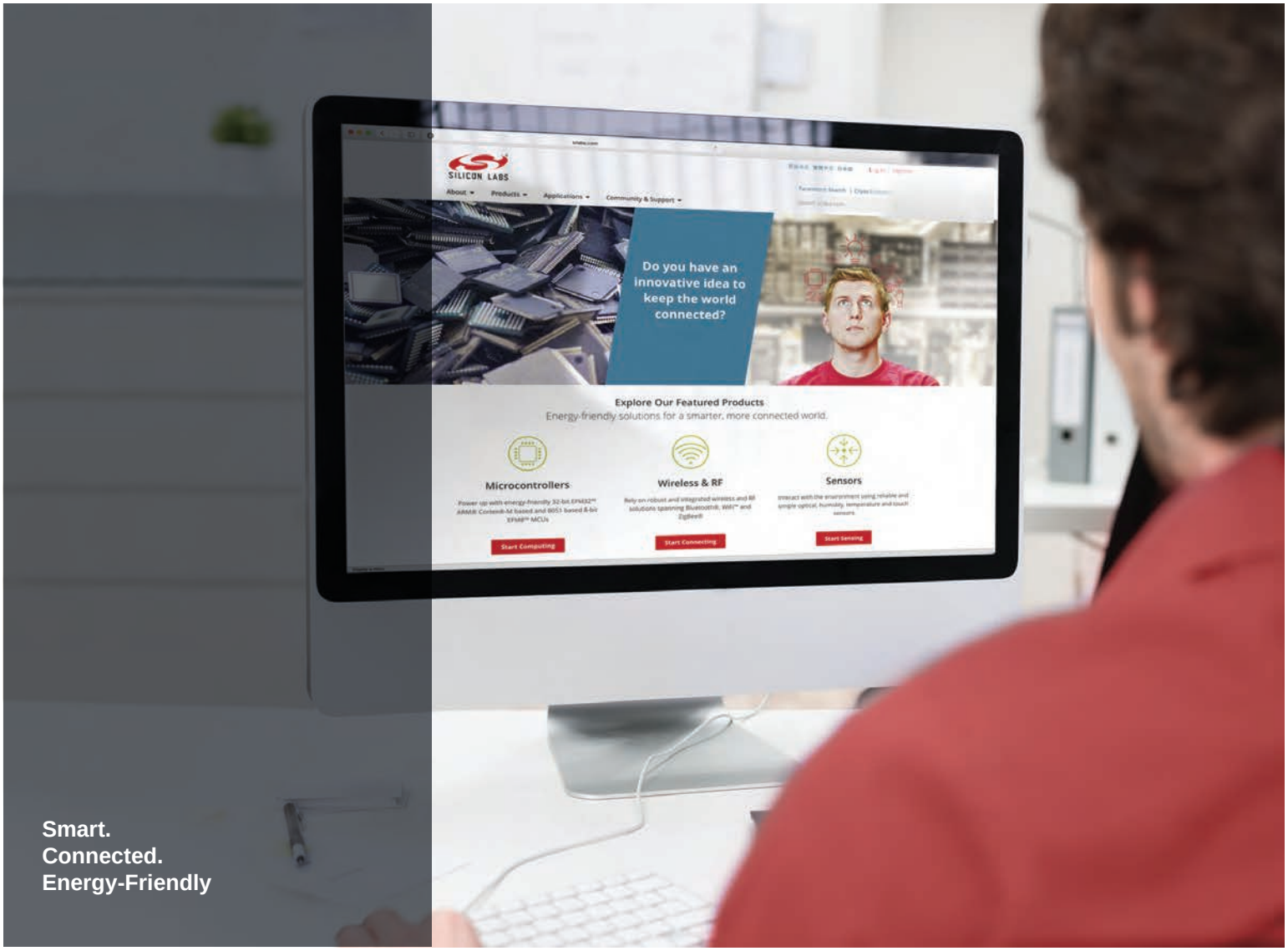

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